Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 1-3 and 6-8 as under 35 U.S.C. § 103(a) as being unpatentable over Seyyedy (U.S. Patent No. 5,926,034) in view of Patel et al. (U.S. Patent No. 6,414,518). Applicant respectfully disagrees.

"The legal concept of prima facie obviousness is a procedural tool of examination which applies broadly to all arts. It allocates who has the burden of going forward with production of evidence in each step of the examination process ... The examiner bears the initial burden of factually supporting a *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness ..." MPEP §2142. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest ***all the claim limitations***. MPEP § 2142 (emphasis added). Here, the references when combined do not teach or suggest all the claim limitations.

"The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art suggests the desirability of the combination." *In re Mills*, 916 F.2d 680; 16 U.S.P.Q. 2d 1430 (Fed. Cir. 1990). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984).

In this case, the Examiner has stated that "with respect to claim 1, figures 3-5 of Seyyedy disclose a programmable I/O circuit comprising: at least one fuse address driver (inherent given that a fuse driver is needed to program the antifuse in figure 5); at least one programmable voltage supply driver (inherent given that the integrated circuit provides several different voltages in the circuit for various standards); programmable output buffers (see figure 3); and means to program the input/output buffers to a desired configuration (the circuit to program the antifuse to have a desired configuration on figure 5). The Examiner goes on to state that though Seyyedy does not specifically show an I/O buffer as claimed, figure 2 of Patel discloses a buffer having both input (2220) and top features for the purpose of delivering and receiving a signal. As set forth below, the references set forth do not teach the claimed invention, let alone all the claim limitations. Applicant's invention and claims pertain to a field programmable gate array.

The Seyyedy patent relates to the manufacture of dynamic static random access memory (DRAM). Laser programmed fuses or other types of programming methods are used to program the DRAM during the final stages of manufacture. For example, fuse options are used to selectively enable columns and/or rows inside a DRAM to replace a defective row with an equivalent functional column or row. This is accomplished during the manufacture of the device. Seyyedy's invention is a DRAM having two buffer circuits as the DRAM output circuit. ***During manufacture***, the fuse options are programmed to select circuits enabling the desired output buffer types. For example, in Col. 1, line 46 Seyyedy states:

"there is a need for reducing differences in the manufacturing process for each memory device with a different logic level interface. There is a further need to apply the process modifications toward the end of the manufacturing process of memory devices to better correlate manufacturing output to demand, which may change quickly"

He further states in Col 2, line 16:

"there is a need to provide the various output levels for semiconductor devices in a manner that makes them easy to manufacture. There is a need to provide modifications of such devices late in the process of making them to ensure that the devices manufactured meet the demand for the various output

levels."

Finally, in Col 3 line 1, Seyyedy states:

"this invention allows for easy selection of a chip's output logic during late stages of manufacture"

It is clear that Seyyedy's invention relates to configuration of output circuits during manufacture and by the manufacturing company and not in the field by the user. In contrast, Applicant's invention teaches I/O circuit configuration in the field by the user, as is needed for field programmable gate arrays (FPGAs). I/O buffer configuration is accomplished by a user programming the FPGA with the circuit required in the field by the user and not at the factory as taught by Seyyedy.

For example, FPGA use, as in Applicant's invention, requires "user selectable" fuse addressing and "user selectable" programmable voltage supply drivers. The "user selectable" fuse addressing and "user selectable" programmable voltage supply drivers are needed because the user may program hundreds of fuses just in the I/O configuration alone. A complex programming scheme is required as illustrated in Applicant's invention.

Seyyedy does not have or need "fuse addressing", instead a reference voltage is simply provided. or a laser programming means is provided because it is "in the factory" and only a few fuses may be blown. The Examiner is mistaken in claiming Seyyedy has antifuse matrix cells when he states that figure 5 of Seyyedy discloses a set of Programmable antifuse matrix cells 534, 536, 538, 540. In fact, these circuits are "output logic circuits and control circuits". Moreover, Seyyedy does not teach how these circuits are selected or programmed.

Patel (6,414,518) teaches a "voltage conversion" scheme. A conversion transistor is used to reduce the voltage used by the internal logic array from that that is generally used at the periphery of the integrated circuit. This allows flexibility in interfacing the circuit with other integrated circuits requiring certain Vcc levels that would otherwise be incompatible with the internal array Vcc. The Patel patent does not relate to Applicant's invention, alone or in combination with Seyyedy.

As to claims 2 through 8, they all depend on claim 1. If an independent claim is found to be non-obvious, all claims depending therefrom are non-obvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596 (Fed. Cir. 1988).

CONCLUSION

For the foregoing reasons, Applicants submit that all of the claims in this application, claims 1 through 8, are in condition for allowance and Applicants respectfully request reexamination of the present application, reconsideration and withdrawal of the present rejections. Should there be any further matter requiring consideration, the Examiner is invited to contact the undersigned counsel.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully submitted,
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